
Detect wire breaks with unusual CMOS gate circuit

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Raju Baddi -February 10, 2014

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Figure 1 Transparent latch using ordinary CMOS gates. Data in is "D" and enable is "E".

A small capacitor is also included at the input which provides noise immunity (either supply or at the input). It also helps to set up timing constraints for the input signals. A transistor is used to latch data into the memory cell. The emitter of the NPN transistor is used to supply the data, and its base terminal is used to control its transmission to the input of the cell. Data is applied to D, and a short positive pulse is applied to E. In a time determined by the RC time constant, this data is copied into the memory cell. Inverter gate based memory cells can provide both non-inverted and inverted outputs while non-inverting gate provides only non-inverted output. The feedback resistor can also be a reverse biased diode, as the input impedance of the gates is very high. A reverse biased diode conducts current on the order of 1nA, which is still two orders of magnitude higher than the input current requirement of the CMOS gate.

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In a bundle of wire with a break somewhere along it, though it is simple to tell whether or not there is a break, it is difficult to pinpoint its location. Using the above discussed memory cell, we shall explore a way of detecting such a break.

In Figure 2a, the broken wire forms a capacitance with a detector cylinder of length 1-3cm through which the wire passes, and charges the input capacitance ($C_i \sim 10\text{pF}$) of G5. The cylinder/wire configuration can have a capacitance on the order of a few pF or less. Hence, to store the required amount of charge on G5's input, a large voltage is required. The opposite ends of the broken wire are connected to out-of-phase square waves of $\sim 30\text{V}$ amplitude. Schematically we have a $\sim 1\text{pF}$ and $\sim 10\text{pF}$ capacitor series combination being charged by a potential difference of 30V (Figure 2b). To toggle the gate, the voltage on its input capacitance C_i should vary on the order of V_T , its input logic threshold voltage. The gates operate at a voltage of only 3V, even though the supply is 25-35V. A 3V supply to

CD4069

/40106 implies a V_T of roughly 1.5V. Even though both the capacitors have the same charge, their voltages are different by a factor of 10 – if the gate input capacitor C_i is charged to $\sim 1.5\text{V}$, the wire-cylinder capacitor C_T is charged to $\sim 15\text{V}$. Thus, a supply of 25-35V is a good choice to generate the square wave signal applied to the two ends of the test wire.

Figure 2 Schematic diagram of wire break detector using CMOS memory cell (shown in broken box). If using the CD40106, only one gate is needed for the oscillator (Schmitt inputs). An additional gate can be put in series with the memory cell G5 and G6 to form a completely separate LED driver. One can directly use a dual color LED if desired as the LEDs can be reversed in orientation simultaneously. Use of bright LEDs and a supply of at least 30V is recommended. It is also possible to use a resistor divider network at the base of Q3 to obtain the 3V supply. When the tube passes over the break, there is a flip in the glow of the LEDs. It should be cautioned that some versions of the

CD4069

might not function properly as an astable due to a low value of V_T .

The square wave is generated using gates G1-G4. The outputs from G3 & G4 control Q1 & Q2 in opposite phase. Gates G5 & G6 form the memory cell which stores the logic state arriving at the input. The LEDs indicate the memory content at the chosen phase of the astable (here, the output of G4). When the tube passes across the break, the LEDs change state.

Figure 3 This shows how the LEDs respond to sleeve position.

Figure 4 Suggested connection for a multiconductor cable.

The detector in action.